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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 09/938,121 | 08/23/2001 | Yoshiyasu Kubota | SONYJP 3.0-204 | 1044 |

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| EXAMINER | |
|---|---|
| YANCHUS III, PAUL B | |
| **ART UNIT** | **PAPER NUMBER** |
| 2116 | |

DATE MAILED: 08/04/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/938,121 | KUBOTA, YOSHIYASU | |
| | Examiner | Art Unit | |
| | Paul B Yanchus | 2116 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *27 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-8* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *1/21/03 & 10/27/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Claim Rejections - 35 USC § 102*

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-8 are rejected under 35 U.S.C. 102(b) as being anticipated by Nakashima, US Patent no. 6,085,982[1].

Regarding claim 1, Nakashima teaches an apparatus [PC Card, 1] adapted for connection to a host system [personal computer, 3] and for receiving electric power [Vcc from personal computer, column 5, lines 36-40] from the host system, the apparatus comprising:

a plurality of function blocks [function 1 and function 2], each function block performing a specified function when selected by the host system [function 1 indicates a modem function and function 2 indicates an ATA memory function, column 4, lines 43-57]; and

a circuit [function-power-source switching control section, 5] operable to control each said function block selected by the host system to consume power at an operating rate and to control each said function block not selected by the host system to consume power at a standby rate less than said operating rate [column 5, lines 25-44].

The Applicant's specification discloses reducing the power consumption of a function block when such block is not selected in order to reduce the power consumption

of an electronic device to a minimum necessary value [paragraph 0052]. Consequently, the claim limitation "to control each said function block not selected by the host system to consume power at a standby rate less than said operating rate" is interpreted to mean that the power consumption of a function block not selected by the host system is to be reduced to a minimum necessary amount.

Nakashima teaches that non-selected function blocks are not required to consume power and further teaches disconnecting power to non-selected function blocks to reduce power consumption of a PC Card to a minimum necessary amount. Therefore, Nakashima discloses the limitation "to control each said function block not selected by the host system to consume power at a standby rate less than said operating rate."

Regarding claim 2, Nakashima further teaches

a function code identifying each of said plurality of function blocks [selection-signal, column 5, lines 10-15]; and

a function register [memory, 16] common to said plurality of function blocks, said function register storing said function code for each said function block selected by the host system, wherein said circuit is operable to control each said function block whose function code is stored in said function register to consume power at said operating rate and to control each said function block whose function code is not stored in said function register to consume power at said standby rate [column 5, lines 25-44 and column 7, lines 30-45].

Regarding claim 3, Nakashima teaches an apparatus [PC Card, 1] adapted for connection to a host system [personal computer, 3] and for receiving electric power

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[1] Included in IDS dated 10/27/03

from the host system [Vcc from personal computer, column 5, lines 36-40], the apparatus comprising:

a plurality of function blocks [function 1 and function 2], each function block performing a specified function when selected by the host system [function 1 indicates a modem function and function 2 indicates an ATA memory function, column 4, lines 43-57];

a function code identifying each of said plurality of function blocks [selection-signal, column 5, lines 10-15];

a circuit [function-power-source switching control section, 5] operable to control each said function block selected by the host system to consume power at an operating rate and to control each said function block not selected by the host system to consume power at a standby rate less than said operating rate [column 5, lines 25-44]; and

a register [memory, 16] common to said plurality of function blocks, said register storing said function code for each said function block selected by the host system and a power save value indicating that a power save mode has been selected by the host system [column 5, lines 25-44 and column 7, lines 30-45];

said circuit being operable to control each said function block whose function code is not stored in said register to consumer power at said standby rate when said power save value is stored in said register [column 5, lines 25-44].

The Applicant's specification discloses reducing the power consumption of a function block when such block is not selected in order to reduce the power consumption of an electronic device to a minimum necessary value [paragraph 0052]. Consequently, the claim limitation "to control each said function block not selected by the host system

to consume power at a standby rate less than said operating rate" is interpreted to mean that the power consumption of a function block not selected by the host system is to be reduced to a minimum necessary amount.

Nakashima teaches that non-selected function blocks are not required to consume power and further teaches disconnecting power to non-selected function blocks to reduce power consumption of a PC Card to a minimum necessary amount. Therefore, Nakashima discloses the limitation "to control each said function block not selected by the host system to consume power at a standby rate less than said operating rate."

Regarding claim 4, Nakashima teaches a data processing system, comprising:

an apparatus for performing at least one function [PC Card, 1]; and

a host system [personal computer, 3] for supplying electric power to said apparatus [Vcc from personal computer, column 5, lines 36-40];

said apparatus including:

a plurality of function blocks [function 1 and function 2], each function block performing a specified function when selected by the host system [function 1 indicates a modem function and function 2 indicates an ATA memory function, column 4, lines 43-57];

a function code identifying each of said plurality of function blocks [selection-signal, column 5, lines 10-15];

a function register[memory, 16] common to said plurality of function blocks, said function register storing said function code for each said function block selected by the host system [column 5, lines 25-44 and column 7, lines 30-45]; and

a circuit [function-power-source switching control section, 5] operable to control each said function block whose function code is stored in said function register to consume power at an operating rate and to control each said function block whose function code is not stored in said function register to consume power at a standby rate less than said operating rate [column 5, lines 25-44]; and

said host system including a writing unit [software, 15] operable to write said function code for each said function block selected by said host system into said function register [column 7, lines 30-45].

The Applicant's specification discloses reducing the power consumption of a function block when such block is not selected in order to reduce the power consumption of an electronic device to a minimum necessary value [paragraph 0052]. Consequently, the claim limitation "to control each said function block not selected by the host system to consume power at a standby rate less than said operating rate" is interpreted to mean that the power consumption of a function block not selected by the host system is to be reduced to a minimum necessary amount.

Nakashima teaches that non-selected function blocks are not required to consume power and further teaches disconnecting power to non-selected function blocks to reduce power consumption of a PC Card to a minimum necessary amount. Therefore, Nakashima discloses the limitation "to control each said function block not selected by the host system to consume power at a standby rate less than said operating rate."

Regarding claim 5, Nakashima teaches a data processing system, comprising:

an apparatus for performing at least one function [PC Card, 1]; and

a host system [personal computer, 3] for supplying electric power to said apparatus [Vcc from personal computer, column 5, lines 36-40];

said apparatus including:

a plurality of function blocks [function 1 and function 2], each function block performing a specified function when selected by the host system [function 1 indicates a modem function and function 2 indicates an ATA memory function, column 4, lines 43-57];

a function code identifying each of said plurality of function blocks [selection-signal, column 5, lines 10-15];

a register [memory, 16] common to said plurality of function blocks, said register storing said function code for each said function block selected by the host system and a power save value indicating that a power save mode has been selected by the host system [column 5, lines 25-44 and column 7, lines 30-45]; and

a circuit [function-power-source switching control section, 5] operable to control each said function block whose function code is stored in said function register to consume power at an operating rate and to control each said function block whose function code is not stored in said function register to consume power at a standby rate less than said operating rate [column 5, lines 25-44].

The Applicant's specification discloses reducing the power consumption of a function block when such block is not selected in order to reduce the power consumption of an electronic device to a minimum necessary value [paragraph 0052]. Consequently, the claim limitation "to control each said function block not selected by the host system to consume power at a standby rate less than said operating rate" is interpreted to mean

controlling the host system to send a notification [selection-signal] to the apparatus identifying the selected function block [column 5, lines 1-25 and column 7, lines 30-45];

controlling power consumption of the plurality of function blocks so that each function block not selected by the host system consumes power at the standby rate of consumption and the selected function block consumes power at an operating rate of consumption greater than the standby rate of consumption [column 5, lines 25-44].

***Conclusion***

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Houston, US Patent no. 6,307,281, teaches selectively supply power to various elements in a computer system.

Ishikawa, US Patent no. 6,266,711 teaches an external unit for adding functionality to a host unit when connected.

Swanberg, US Patent no. 5,832,280, teaches modifying the power mode of a device using power mode select registers.

Kikinis et al., US Patent no. 5,821,924, teaches lowering the power consumption of a peripheral component when the peripheral is inactive.

Moyer, US Patent no. 5,689,714, teaches a method of setting a peripheral device to a low power mode by writing status values to special registers.

controlling the host system to send the function code [selection-signal] of the selected function block to the apparatus [column 5, lines 1-25 and column 7, lines 30-45];

controlling the apparatus to set the function code of the selected function block to the register [memory, column 7, lines 30-45]; and

reading the function code of the selected function block from the register and controlling power consumption of the plurality of function blocks so that the selected function block consumes power at an operating rate of consumption greater than said standby rate of consumption and each said function block whose function code is not stored in the register consumes power at said standby rate of consumption [column 5, lines 25-44].

Regarding claim 8, Nakashima teaches a data processing system including a host system [personal computer, 3] and an apparatus [PC Card, 1] for performing functions, the apparatus including a plurality of function blocks [function 1 and function 2], each function block performing a specified function when selected by the host system [function 1 indicates a modem function and function 2 indicates an ATA memory function, column 4, lines 43-57], and a method of controlling power consumption of the apparatus, comprising:

supplying electric power from the host system to each of the plurality of function blocks at a standby rate of consumption [Vcc from personal computer, column 5, lines 36-40];

operating the host system to select a function block from among the plurality of function blocks [column 5, lines 1-25 and column 7, lines 30-45];

that the power consumption of a function block not selected by the host system is to be reduced to a minimum necessary amount.

Nakashima teaches that non-selected function blocks are not required to consume power and further teaches disconnecting power to non-selected function blocks to reduce power consumption of a PC Card to a minimum necessary amount. Therefore, Nakashima discloses the limitation "to control each said function block not selected by the host system to consume power at a standby rate less than said operating rate."

Regarding claim 6, Nakashima teaches that the host system includes a writing unit [software, 15] operable to write said function code for each said function block selected by said host system and said power save value into said register [column 7, lines 30-45].

Regarding claim 7, Nakashima teaches a data processing system including a host system [personal computer, 3] and an apparatus [PC Card, 1] for performing functions, the apparatus including a plurality of function blocks [function 1 and function 2] and a register [memory, 16] common to the plurality of function blocks, each function block performing a specified function when selected by the host system [function 1 indicates a modem function and function 2 indicates an ATA memory function, column 4, lines 43-57], and a method of controlling power consumption of the apparatus, comprising:

supplying electric power from the host system to each of the plurality of function blocks at a standby rate of consumption [Vcc from personal computer, column 5, lines 36-40];

operating the host system to select a function block from among the plurality of function blocks [column 5, lines 1-25 and column 7, lines 30-45];

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul B Yanchus whose telephone number is (703) 305-8022. The examiner can normally be reached on Mon-Thurs 8:00-6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne H Browne can be reached on (703) 308-1159. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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Paul Yanchus
July 26, 2004